After obtaining this basic design, we ran simulations and made adjustments to the stages in order to meet the specs. The first simulation that we ran that met the gain specification can be seen in figure 10. This yielded a gain of 5.71E6 V/A, which is within the specified 5E6 and 10E6 V/A.

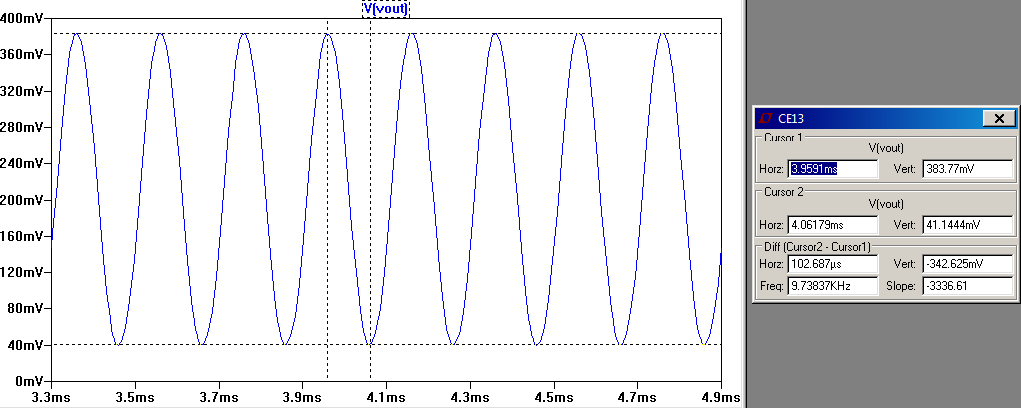
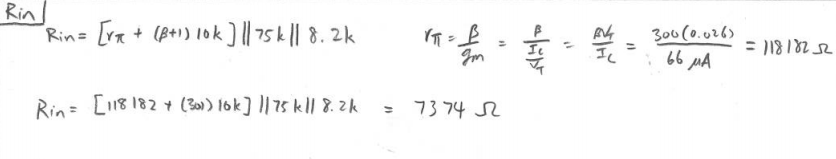


Figure 10 simulated gain

Using the schematic values we were able to calculate the capacitors needed to achieve our upper and lower corner frequencies. In order to calculate the capacitors needed for the lower corner frequency, we first had to calculate the Rin of the CE BJT. The calculations for the Rin of the CE BJT and the lower corner frequency can be seen in figure 11.



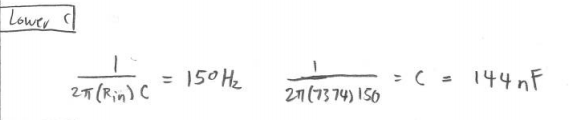


Figure 11 calculations for Rin and lower corner frequency

The upper frequency can be determined by using the resistor value between the collector of the CE BJT and Vcc. The calculation for the capacitor value needed to achieve our upper corner frequency can be seen in figure 12.

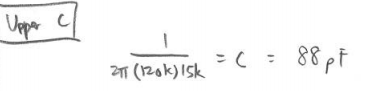


Figure 12 calculation for upper corner frequency

Using these capacitor values we were able to run simulations. We needed to slightly adjust our calculated capacitances in order for our corner frequencies to be where we want them to be. We ultimately adjusted the capacitance for the lower corner frequency to be 165nF and the capacitance for our upper corner frequency to be 140 pF. The simulation for the lower and upper corner frequency can be seen in figure 13 and 14 respectively.

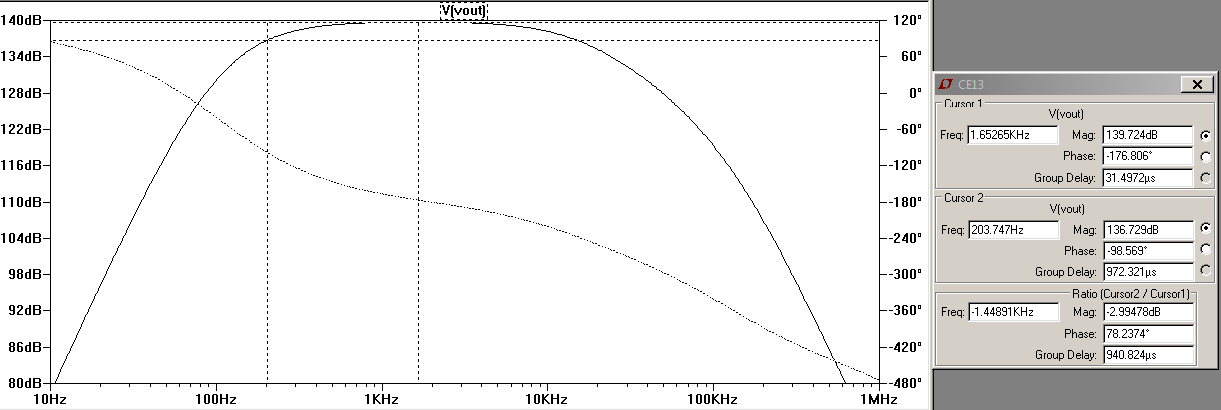


Figure 13 lower corner frequency

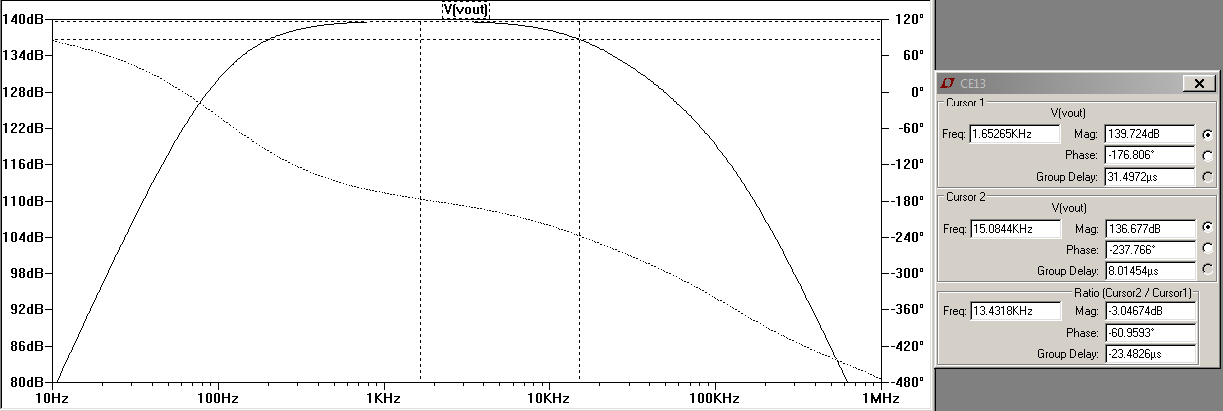


Figure 14 upper corner frequency

Now that we have a circuit that meets some of the specifications, we need to make sure that it meets the specification for output impedance. The calculations for the output impedance of the circuit can be seen in figure 15.

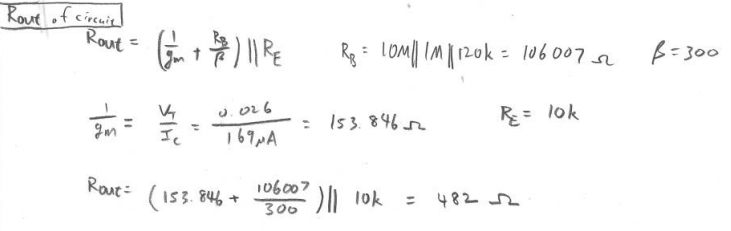


Figure 15 output impedance of the whole circuit

In order to test the power consumption of our circuit, we put a 20 nA input and then a 100 µA input to see if either one of them drew too much power from the power source. The simulations for both can be seen in figure 16 and 17 respectively.

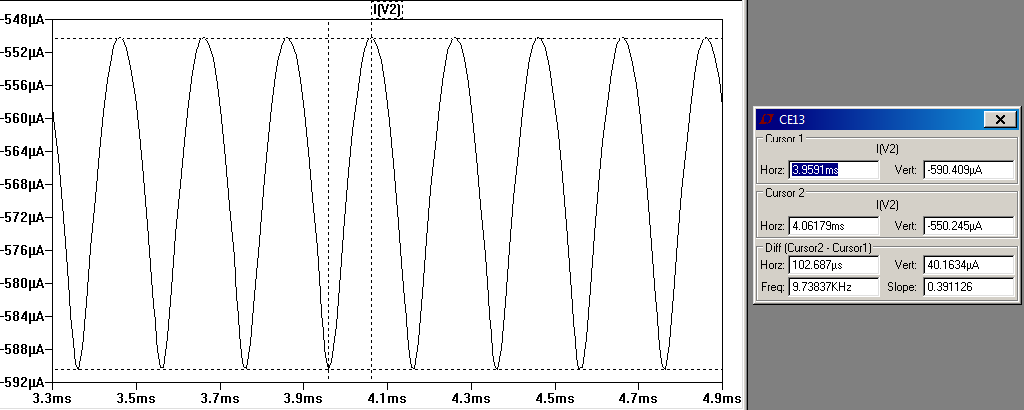


Figure 16 power consumption at 20 nA

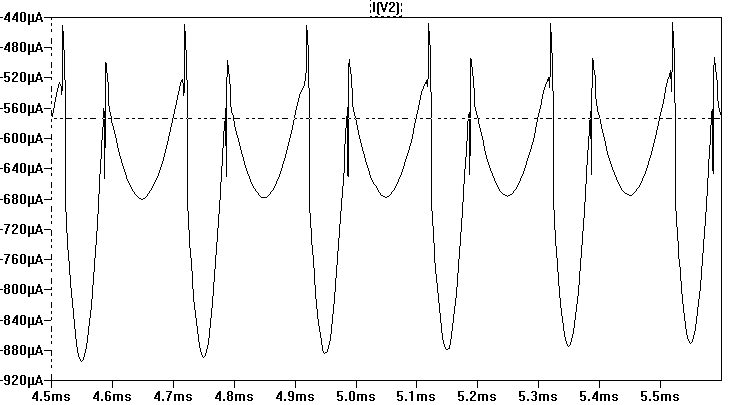


Figure 17 power consumption at 100 µA

Now that we have a complete schematic that works in theory, we started building our circuit on the breadboard. As we went along, we ran into problems and found ways to solve them. Most of them involved changing the circuit resistors. These changes will be mentioned later when we go into detail about building the circuit on the breadboard. After all the tuning we have our final schematic (figure 18).

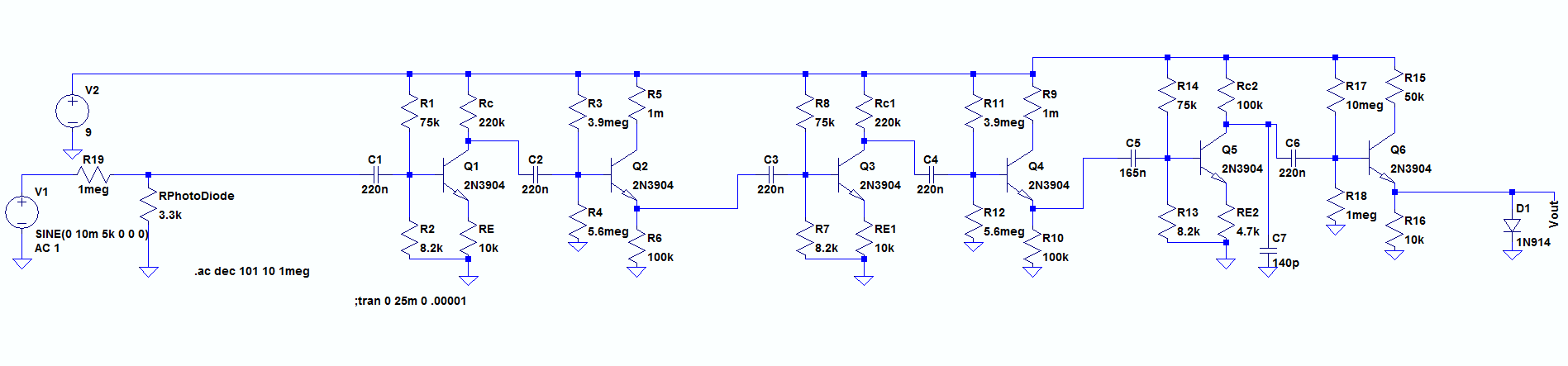


Figure 18 final LTSpice schematic

After building the circuit on the breadboard, we began testing. We first tried to measure the gain across the first two stages. The output voltage (figure 2) divided by the input voltage (figure 3) equaled 280.5.



Figure 2 output voltage across two stages

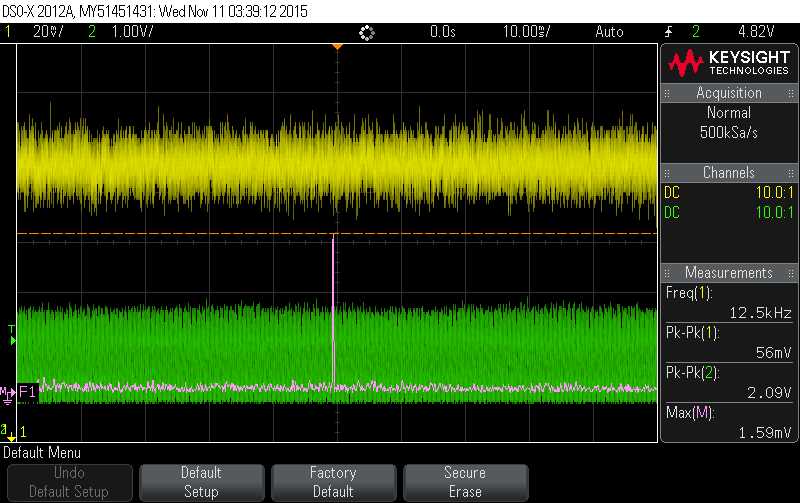


Figure 3 input voltage across two stages

We then tried to measure the gain across all three stages. The output (figure 4) divided by the input (figure 5) equaled 280. This was definitely well below the gain that we were aiming for. However, we can see from the output voltage that there is a considerable amount of clipping going on.

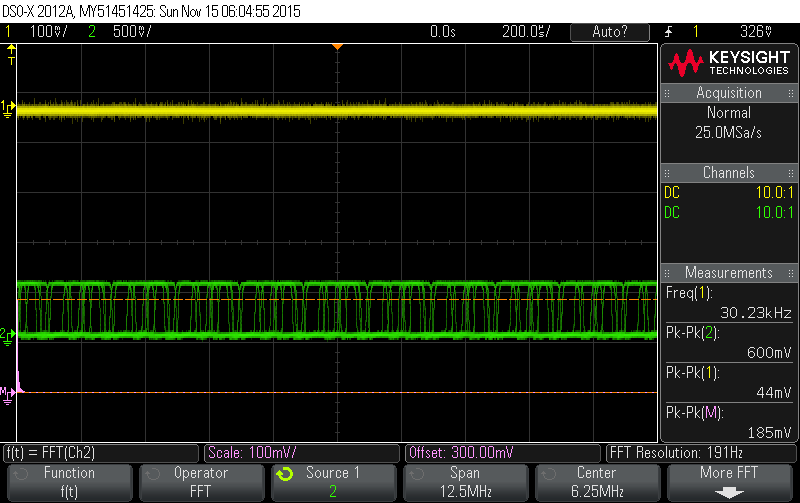


Figure 4 output voltage across three stages without diode

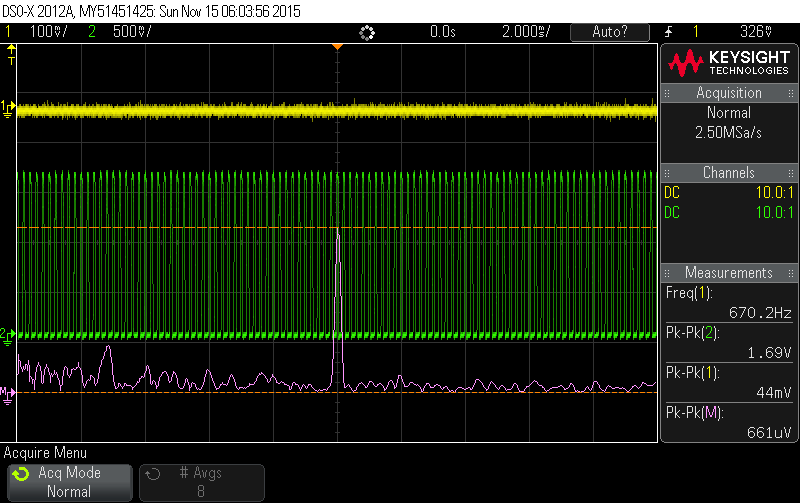


Figure 5 input voltage across three stages

We saw that there was basically no gain across the third stage. After closer inspection and some calculations, we noticed that the final CE BJT was in saturation. We had to change the 120kΩ on the final CE stage to a 100kΩ resistor, because the LTSpice simulation had not taken into account the state of the BJT. Because of the change on that resistor we had to recalculate the capacitor value needed to achieve the upper corner frequency as well.

With the redesigned circuit we again measured the gain at 2 kHz, which should have no attenuation. The output voltage (figure 6) divided by the input voltage (figure 7) equaled 8.63. We had the MΩ resistor at the beginning of the circuit, so this would be equivalent to 8.63 million V/A gain, which meets the specs.



Figure 6 output voltage @ 2 kHz

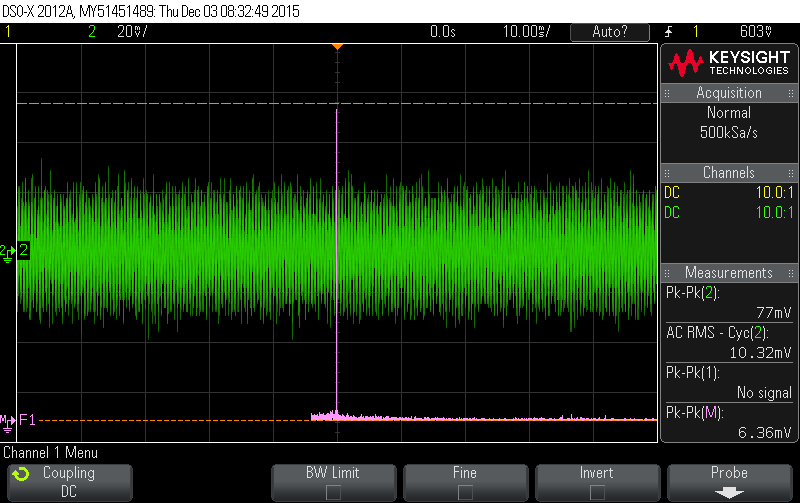


Figure 7 input voltage @ 2kHz

Using the oscilloscope we were able to determine our lower corner frequency to be 280 Hz (figure 8) and our upper corner frequency to be 10.9 kHz (figure 9). These were relatively close to our calculations that yield a lower frequency of 170 Hz and an upper frequency of 10.9 kHz.

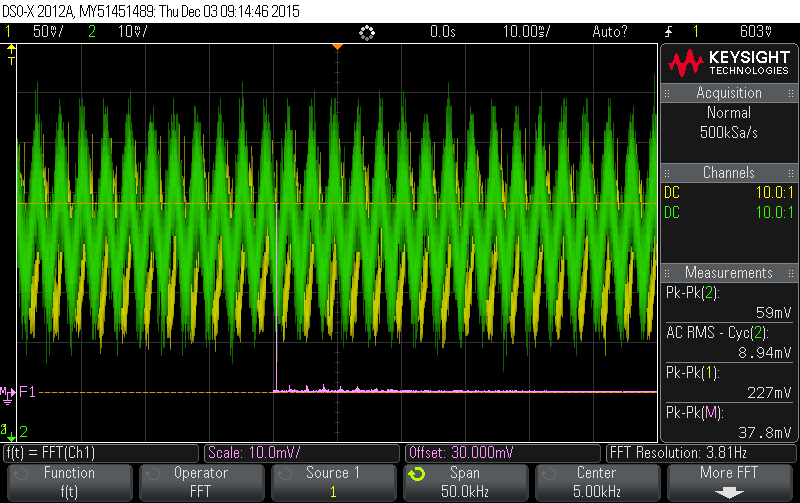


Figure 8 lower corner frequency - 280 Hz



Figure 9 upper corner frequency - 10.9 kHz

After the tests on our corner frequencies, we measured our power consumption. Within a reasonable input voltage we saw that the maximum power consumption from the battery is around 0.66 mA.

-Talk about breadboarding. We built stages at a time

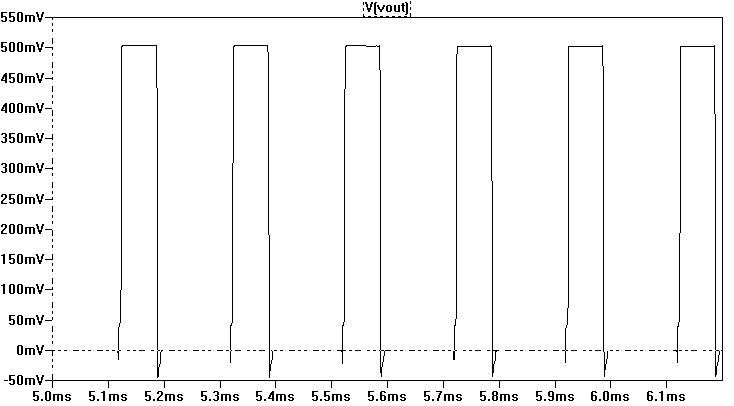
-Talk about 3rd CE stage saturation

Output impedance calculations

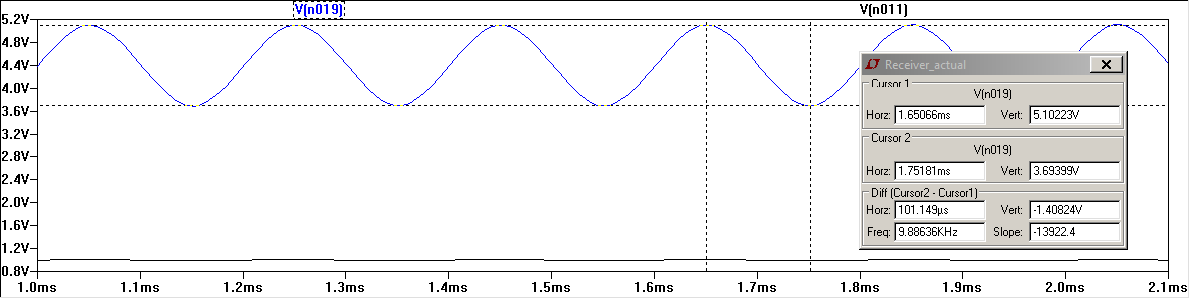
Power consumption 20nA

Power consumption 100uA

Output limiting at 100uA

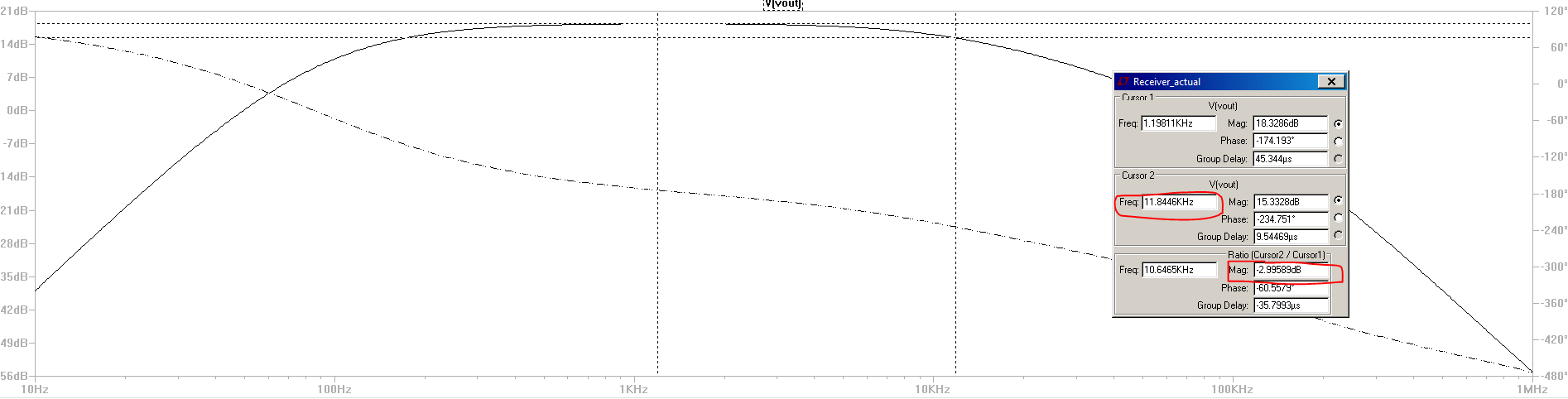


Testing 2 stages

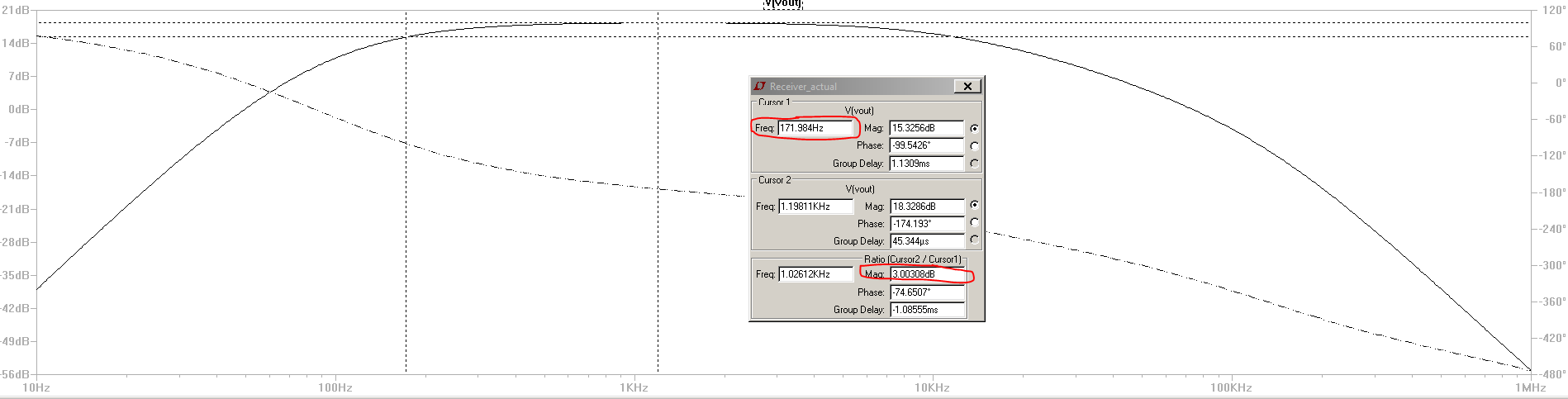


Final Schematic

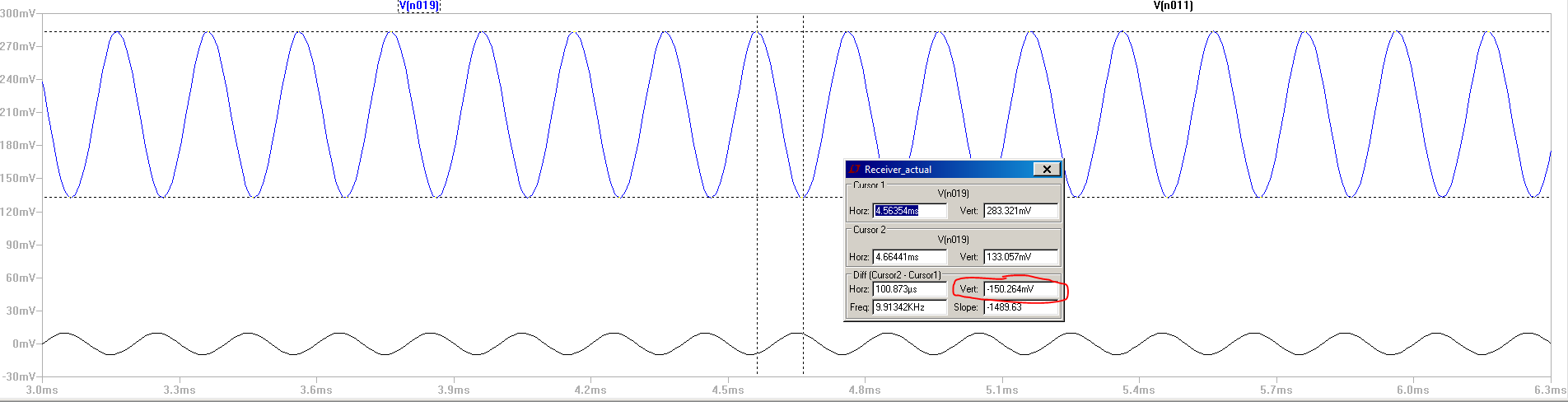
Final Upper corner freq



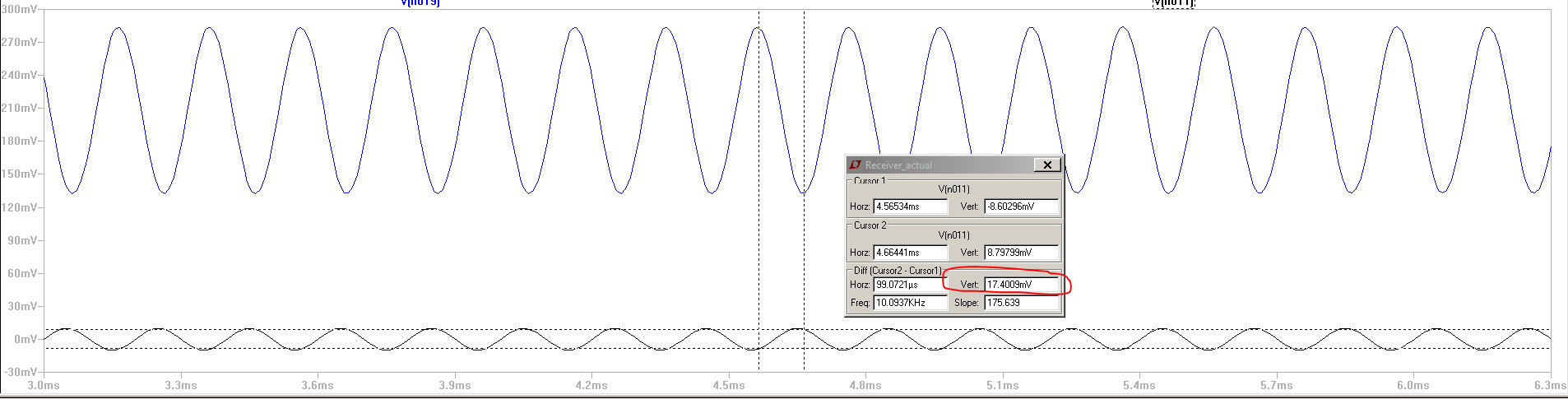
Final lower corner freq



Final gain – output



Final gain input



Final current draw

